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Objectives

- Seeking an internship in the Bay Area to leverage my technical skills and academic background in digital design, verification, and energy efficiency for impactful contributions to innovative projects.
- A versatile Electrical and Computer Engineer with expertise in digital design, SystemVerilog, and energy-efficient systems, aiming to contribute innovative solutions to advanced industrial and technological projects.
- Proficient in designing and verifying digital architectures, including ASIC implementations and robust embedded systems, with a strong focus on functional verification and performance optimization.
- Skilled in conducting energy efficiency audits and optimizing industrial processes, delivering actionable, data-driven recommendations to enhance sustainability and reduce operational costs.

Educational Background

Master of Science in Electrical and Computer Engineering
San Francisco State University (SFSU) - GPA: 4.00/4.00 (Spring 2026)

Bachelor of Science in Electrical Engineering – Minor in Electronics Systems (ESET)
Iran University of Science and Technology (Sep 2017-May 2022)
Tehran | Iran - GPA: 3.7 / 4.00

Key Courses

- Advance Digital Design – Digital Design Verification – Embedded Systems – ASIC Design (SFSU)
- Logic Circuits – Microprocessors - Computer Systems (IUST)
- Machine Learning & python programing online courses at Stanford University | Coursera

Professional Skills

- Solid understanding of **Analog** and **Mixed-Signal** circuits, **IC Test and Validation**, **PCB design**, Signal Integrity/Power Integrity, schematic entry, **SPICE simulation**. Experience with scripting/algorithm development for data processing.
- Expertise in ASIC/SoC design, verification and integration, **digital logic design** in advanced technology nodes, **UVM environment**, Design for Testability (DFT), Physical Design (PnR), Static Timing Analysis (STA), RTL-to-GDSII Flow, Low Power Optimization. Proficient in Synopsys & Cadence Tools.
- Languages: C, C++, Python, Verilog, SystemVerilog, VHDL, Tcl, Perl, Linux.

HSPICE / NGSPICE	Microcontrollers	Synopsys ICC2
Xilinx Vivado	Altium Designer	Siemens Questa
Synopsys Design Compiler	STM/Raspberry pi	MATLAB and Simulink

Relevant Projects

- **ASIC Implementation of motion estimator in 14nm FinFET Technology**
  - Implementing and Design of Motion Estimator with 16x16 reference block and 32x32 search block.
  - Verified RTL starting from front-end synthesis, timing check followed by back-end physical design.
  - Verified the layout of the design using DRC as a part of the physical design sign-off.
- **16×8 SRAM in 14nm CMOS Technology | VLSI System Design (6T SRAM Design)**
  - Designed a **custom SRAM architecture** from scratch in advanced **CMOS technology**, **optimizing area, access time, and power efficiency.**
  - Developed and verified the **read/write operation circuitry**, ensuring robust performance and signal integrity under worst-case conditions.
  - Performed **DRC and LVS** checks to validate design rule compliance and layout-versus-schematic consistency.
  - Conducted **comprehensive functional verification** and power characterization using **Synopsys Custom Compiler**, ensuring design reliability through structured read/write test sequences.
- **Teradyne J750 Training & Device Setup – Nano Electronics & Computing Research Laboratory (SFSU)**
  Trained by a Teradyne expert during on-campus installation of the J750 semiconductor test system
  - Completed step-by-step hands-on training on operating the J750, including test procedures, system configuration, and hardware/software integration.
  - Authored a comprehensive technical report documenting the J750's specifications, capabilities, and setup process—serving as the primary deliverable for the training.
  - Assisted with initial system calibration during the installation process.

Work Experiences

Energy Engineer
(Sep 2024 – April 2025)

United States

SFSU Industrial Assessment Center (IAC) – Part time

- Conduct on-site energy efficiency audits for manufacturing and water/wastewater treatment facilities funded by the DOE and supported by PG&E.
- Perform data analysis and develop detailed reports outlining energy-saving recommendations, including engineering and economic analyses.
- Identify and propose solutions for Energy Conservation Opportunities (ECOs), Waste Minimization Opportunities (WMOs), Water Conservation Opportunities (WCOs), and Productivity Improvement Opportunities (PIOs).
- Provide actionable recommendations for renewable generation, cogeneration, and operational cost reduction.
- Support sustainable industrial practices through no-cost assessments and confidential reporting, helping businesses improve efficiency and reduce energy consumption.

Internship
(Duration: 6 Months)

Iran University of Science and Technology
Machine Vision Laboratory, supervised by Dr. Shahriyar Baradaran Shokouhi

- Responsibilities: Optimizing machine learning algorithms and neural networks for computer vision applications. Conducted research on advanced image processing techniques and state-of-the-art neural network architectures, including CNNs, RNNs, GANs, and transformer models. Implemented and tested models using Python, TensorFlow, Keras, and OpenCV. Collaborated with researchers to enhance algorithm performance, focusing on accuracy, efficiency, and real-time processing. Contributed to research papers, technical documentation, and presentations.

Research Assistance
(Sep 2024 – Present)

San Francisco State University - SFSU

- Utilized machine learning algorithms to determine optimal delay models (L model, Pi model, Double Pi model), identifying the model with the minimal delay for improved future performance and application.
- Designed an efficient algorithm to improve delay estimation by accurately modeling the driving-point admittance of RC-tree structures, accounting for the influence of series resistance on on-chip interconnects.
- Enhanced the accuracy of delay predictions through a detailed analysis of voltage-transfer ratios in RC-tree models, leading to better performance in gate-driving applications using an ECL clock buffer as a case study.

Teaching Assistant

San Francisco State University – SFSU
(Sep 2024 - Dec 2024)*

- Digital Design System / Laboratory*
- Control Systems*
- Computer Systems*
- Linear System Analysis**
- Operational Amplifier System Design**
- Communication Systems**

(Jan 2025 - Present)**

Teaching Assistant

Iran University of Science and Technology - IUST

- Logic Circuit Design

(Duration: 6 Months)

General Skills

- An innovative mindset and ability to generate and work with new ideas, technologies, tools and techniques.
- Excellent analytical and synthesis skills, with great attention to detail.
- Ability to manage priorities and work on multiple projects simultaneously.
- Ability to work in a team with a positive and professional attitude.
- Self-motivated individual, innovative, confident, thorough and team oriented.

Publications

- **Designing and implementing a real-time intelligent system for object identification and classification**
  Seventh International Conference on Technology Development in Iranian Electrical Engineering | (19 June 2022, Tehran, I. R. IRAN)